I claim:

1. A system comprising:

a frame buffer memory for a serially addressable, non-direct memory access (DMA) display, the frame buffer memory having a number of pixels corresponding to a number of pixels of the non-DMA display; and,

a display data transfer circuit to serially transfer the pixels of the frame buffer memory to the non-DMA display to update the non-DMA display.

2. The system of claim 1, further comprising the non-DMA display.

3. The system of claim 1, wherein the non-DMA display is communicated with via a communication format comprising:

an x coordinate of the display;

a y coordinate of the display; and,

a number of sequential pixels to be written to the display starting at the x coordinate and at the y coordinate.

4. The system of claim 1, wherein the non-DMA display is one of a stand-alone display and an embedded display.

5. The system of claim 1, wherein the frame buffer memory is separate from the display data transfer circuit.

6. The system of claim 1, wherein the frame buffer memory is part of the display data transfer circuit.

7. The system of claim 1, wherein the data transfer circuit is an application-specific integration circuit (ASIC).

8. The system of claim 1, wherein the frame buffer memory has a bit depth of at least one bit corresponding to a bit depth of the display.

9. The system of claim 1, wherein the display data transfer circuit is to start at an origin point of the display when serially transferring the pixels of the frame buffer memory to the display.

10. The system of claim 1, wherein the display data transfer circuit is to monitor changes made to the pixels of the frame buffer memory, and is to serially transfer the pixels of the frame buffer memory that have changed to the display.

11. The system of claim 10, wherein the display data transfer circuit is to serially transfer the pixels of the frame buffer memory that have changed to the display by determining a number of sequential pixel groups inclusive of one or more of the pixels of the frame buffer memory that have changed that minimize data transfer to the display.

12. The system of claim 11, wherein at least one of the sequential pixel groups are also inclusive of one or more of the pixels of the frame buffer memory that remain unchanged.

13. The system of claim 10, wherein the frame buffer memory is a first frame buffer memory, the system further comprising a second frame buffer memory to which the pixels of the first frame buffer memory are copied, the display data transfer circuit to compare pixels of the second frame buffer memory against the pixels of the first frame buffer memory to determine whether changes have been made to the pixels of the first frame buffer memory.

14. The system of claim 10, further comprising a mask to indicate that changes have been made to the pixels of the frame buffer memory.

15. The system of claim 1, wherein the frame buffer memory supports at least one of an endianness selector and a bit directional selection capability.

16. A system comprising:

a frame buffer memory for a serially addressable, non-direct memory access (DMA) display, the frame buffer memory having a number of pixels corresponding to a number of pixels of the non-DMA display; and,

means for serially transferring the pixels of the frame buffer memory to the non-DMA display to update the non-DMA display.

17. The system of claim 16, further comprising the non-DMA display.

18. The system of claim 16, wherein the non-DMA display is communicated with via a communication format comprising:

an x coordinate of the display;

a y coordinate of the display; and,

a number of sequential pixels to be written to the display starting at the x coordinate and at the y coordinate.

19. The system of claim 16, wherein the means is further for monitoring changes made to the pixels of the frame buffer memory, and for serially transferring the pixels of the frame buffer memory that have changed to the non-DMA display as a series of pixel groups.

20. The system of claim 19, wherein each pixel group includes one or more sequential pixels of the frame buffer memory that have changed.

21. The system of claim 19, wherein each pixel group includes a sequence of at least one pixel, the sequence of at least one pixel group including one or more of the pixels of the frame buffer memory that remain unchanged.

22. A method comprising:

determining that one or more pixels of a frame buffer memory for a serially addressable, non-direct memory access (DMA) display have changed; and,

in response to determining that the one or more pixels of the frame buffer memory have changed, serially transferring at least the one or more pixels from the frame buffer memory to the display.

23. The method of claim 22, wherein determining that the one or more pixels of the frame buffer memory have changed comprises comparing the frame buffer memory to a previously made copy of the frame buffer memory to determine whether one or more pixels of the frame buffer memory have changed.

24. The method of claim 22, wherein determining that the one or more pixels of the frame buffer memory have changed comprises utilizing a mask indicating that the one or more pixels have changed.

25. The method of claim 22, wherein serially transferring at least the one or more pixels from the frame buffer memory to the display comprises, for each pixel of the one or more pixels,

specifying to the display an x coordinate and a y coordinate of the pixel; and,

specifying the pixel to the display.

26. The method of claim 22, wherein serially transferring at least the one or more pixels from the frame buffer memory to the display comprises determining a number of sequential pixel groups inclusive of at least the one or more pixels that minimize data transfer to the display.

27. The method of claim 26, wherein determining the number of sequential pixel groups comprises determining at least one pixel group that is also inclusive of one or more pixels of the frame buffer memory that remain unchanged.

28. The method of claim 26, wherein serially transferring at least the one or more pixels from the frame buffer memory to the display further comprises, for each sequential pixel group,

specifying to the display an x coordinate and a y coordinate at which the sequential pixel group starts; and,

specifying to the display a number of bits corresponding to the sequential pixel group.

29. A printing device comprising:

a printing mechanism by which the printing device is able to print images onto media;

an embedded serially addressable, non-direct memory access (DMA) display by which a user is able to monitor the printing mechanism and change characteristics of the printing mechanism;

a frame buffer memory for the embedded display, the frame buffer memory having a number of pixels corresponding to a number of pixels of the embedded display; and,

a display data transfer circuit to serially transfer the pixels of the frame buffer memory to the embedded display to update the embedded display.

30. The device of claim 29, wherein the embedded display is communicated with via a communication format comprising:

an x coordinate of the display;

a y coordinate of the display; and,

a number of sequential pixels to be written to the display starting at the x coordinate and at the y coordinate.

31. The device of claim 29, wherein the display data transfer circuit is to serially transfer the pixels of the frame buffer memory to the display by monitoring changes made to the pixels of the frame buffer memory and serially transferring the pixels of the frame buffer memory that have changed to the display.

32. The device of claim 29, wherein the display data transfer circuit is to serially transfer the pixels of the frame buffer memory to the display by determining a number of sequential pixel groups inclusive of one or more pixels of the frame buffer memory that have changed that minimize data transfer to the display.

33. The device of claim 29, wherein the printing mechanism is one of a laser-printing mechanism and an inkjet-printing mechanism, such that the printing device is one of a laser-printing device and an inkjet-printing device.